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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/709,138 | 04/15/2004 | Kei MURAYAMA | 040170 | 3137 |

23850 7590 07/20/2007
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| EXAMINER | |
|---|---|
| BAREFORD, KATHERINE A | |
| ART UNIT | PAPER NUMBER |
| 1762 | |

| MAIL DATE | DELIVERY MODE |
|---|---|
| 07/20/2007 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/709,138 | MURAYAMA, KEI | |
| | Examiner | Art Unit | |
| | Katherine A. Bareford | 1762 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *05 June 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,7 and 9-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Claims 2, 5, 6, 8 and 12 are canceled

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Continued Examination Under 37 CFR 1.114*

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on June 5, 2007 has been entered.

The after final amendment of May 23, 2007 has been entered as required by the RCE submission. With the entry of the amendment, claims 2, 5, 6, 8 and 12 are canceled, and claims 1, 3, 4, 7 and 9-11 are pending for examination.

### *Claim Objections*

2. Claims 3, 4, 7, 9 and 10 are objected to because of the following informalities: each of these claims begins with "An electroless plating method according to claim 1 . . ." or "An electroless plating method according to claim 11 . . .". However, independent claims 1 and 11 have been amended in the preamble to read "A method of manufacturing a wiring substrate . . .", and therefore the preambles of claims 3, 4, 7, 9 and 10 should be amended to reflect this.

Appropriate correction is required.

*Claim Rejections - 35 USC § 112*

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1, 3, 4, 7 and 9-11 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Independent claim 1, lines 15-16 has been amended to read ". . . thereby, the step of forming a solder resist pattern on the space portion is omitted by forming the oxidizing agent". Independent claim 11, lines 14-15 has been amended to read ". . . thereby, the step of forming a solder resist pattern on the space portion is omitted by forming the oxided agent". Applicant has not provided where in the application as originally filed support for such an amendment is provided. The Examiner has reviewed the disclosure as originally filed and finds no teaching of specifically omitting formation of a solder resist pattern. Therefore, it is new matter to claim the negative limitation of omitting formation of a solder resist pattern. The Examiner notes that as worded claim 11 is further not supported because as discussed in the 35 USC 112,

second paragraph rejection the claim is directed to forming a "protection film" not applying oxidizing/oxidized agent.

The other dependent claims do not cure the defects of the claims from which they depend.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1, 3, 4, 7 and 9-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1, lines 12-15, claims ". . . the distance between the electrodes of the conductive pattern in the space portion between the electrodes has a plurality of different values, the oxidizing agent is selectively coated in the space portions which are smaller than . . " This is confusing as worded, because "the space portion" as originally referred to refers to ALL the space between electrodes, as the "distance between electrodes in the space portion . . . has a plurality of different values" and in the later use of "the space portions" apparently individual areas and distances are referred to.

Claim 11, lines 11-14, claims ". . . the distance between the electrodes of the conductive pattern in the space portion between the electrodes has a plurality of different values, the oxidizing agent is selectively coated in the space portions which are

smaller than . . " This is confusing as worded, because "the space portion" as originally referred to refers to ALL the space between electrodes, as the "distance between electrodes in the space portion . . . has a plurality of different values" and in the later use of "the space portions" apparently individual areas and distances are referred to.

Claim 11, lines 14-15, claims "the oxidizing agent is selectively coated in the space portions which are smaller than . . . the step of forming a solder resist pattern . . . by forming the oxidized agent." This is confusing as worded because "the oxidizing agent" and "the oxidized agent" lack antecedent basis and conflict with the earlier parts of the claim which involve selectively forming "a protection film" in "a space portion between the conductive pattern." Because of this confusion, for purposes of examination, the Examiner is treating claim 11, lines 14-15 as intending to refer to "the protection film" where "oxidizing agent" and "oxidized agent" is referred to. It is also unclear how the "protection film" which can be a resist film (claim 9) differs from the described "solder resist".

The other dependent claims do not cure the defects of the claims from which they depend.

### *Claim Rejections - 35 USC § 103*

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1, 3, 4, 7 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al (US 5167992) in view of the admitted state of the prior art, EP 837 623 (hereinafter '623) and Miller (US 4668533).

Lin teaches a method of electroless plating. Column 1, lines 5-10. A substrate is prepared that has an insulating body and a conductive pattern formed on the insulating body. Column 3, lines 45-55 and column 4, lines 30-50. The substrate is to be used for microelectronic interconnect substrates or circuit boards. Column 3, lines 45-55. A catalytic metal serving as a catalyst of an electroless plating process is adhered onto the insulating body and the conductive pattern. Column 5, lines 35-60. An oxidizing agent, which can oxidize the catalytic metal and make the catalytic metal in an inactive state to the electroless plating is applied to the catalytic metal. Column 5, line 60 through column 6, line 20 and column 7, lines 25-35. It would be applied in a space portion S between the conductive pattern features (as it is shown being applied to the entire surface). Column 5, line 60 through column 6, line 20. Then a metal layer is selectively formed on the conductive pattern by electroless plating. Column 6, lines 20-30.

Claim 4: the adhering of the catalytic metal onto the insulating body and the conductive pattern includes coating an activating solution containing ions of the

catalytic metal to deposit the catalytic metal by an oxidation reduction reaction. Column 5, lines 50-60 and column 7, lines 20-25.

Claim 7: the catalytic metal is palladium. Column 5, lines 45-60. The metal formed by electroless plating can be a nickel layer. Column 6, lines 20-40.

Claim 10: the oxidizing agent can be sulfuric acid ($H_2SO_4$). Column 7, lines 20-30.

Lin teaches all the features of these claims except that (1) the conductive pattern includes electrodes to be used with connection pads, (2) the space portion between the electrodes has a plurality of different values, (3) that the oxidizing agent is coated selectively so that the oxidizing agent is formed selectively in portions, which are smaller than 30 microns, out of the space portion between the electrodes, (4) the ink jet application of the oxidizing agent (claim 3).

The admitted state of the prior art teaches that when forming wiring substrates with conductive patterns, it is well known for the wiring patterns to include electrodes formed of copper which then are overplated to enhance reliability, and the electrodes form connections to the electronic parts. See paragraphs [0002] – [0008] of the specification. It is also well known for the pitch of the copper electrodes on the wiring substrate to be narrowed to 60 microns or less. See paragraph [0004] of the specification. It is also well known for the space portions between the copper electrodes to vary over the substrate. See paragraph [0006] of the specification. It is also well known to desire to form a nickel layer selectively on the copper electrodes by electroless plating. See paragraphs [0002] – [0008] of the specification.

'623 teaches that it is well known to overplate by electroless plating selectively over conductive patterns on a insulating substrate when making printed circuit boards, for example. Column 1, lines 1-10 and column 4, lines 35-45. The overcoating can be nickel based resistors. Column 7, lines 1-15. '623 provides providing a conductive circuit pattern on the insulating substrate. Column 4, lines 35-55. Then the surfaces of the conductive pattern and the substrate are activated. Column 4, lines 50-55 and column 6, lines 30-45. Then '623 provides applying a plating mask onto the activated substrate so that the areas to be plated are defined in a negative manner, where the plating mask covers all or substantially all of the surfaces except for the resistor areas to be plated. Column 6, lines 45-55. The area to be plated can be partially over the conductive pattern and partially over the insulating substrate. Column 6, lines 50-56. Then, electroless plating occurs, with plating occurring only on the areas not covered by the mask. Column 7, lines 1-15. The exact size of the resistor area to be plated can vary. Column 7, lines 20-30.

Miller teaches ink jet printing as a method to apply materials for electroless plating in a selective form, such as the sensitizers and activators. Column 2, lines 40-50, column 3, lines 45-60 and column 4, lines 15-30. The substrate can be an active integrated circuit. Column 3, lines 25-35.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to (1), (2) ~~and (5)~~ modify Lin to provide that the conductive pattern includes electrodes spaced different distances apart and that these electrodes can be less

than 60 microns apart as suggested by the admitted state of the prior art in order to provide a desirable circuit and microelectronic pattern because Lin teaches forming conductive patterns on insulating substrates for circuit and microelectronic usage, and the admitted state of the prior art teaches that conductive patterns on wiring substrates for such purposes conventionally have copper electrodes spaced different distances apart and that the electrodes can be less than 60 microns apart. It further would have been obvious to perform routine experimentation to optimize the distance apart to less than 30 microns apart in at least some cases as the admitted state of the prior art provides that less than 60 microns apart is conventional, and 30 microns is included in the range of less than 60 microns. As to the electrodes being on which connection pads of an electronic part are connected, the admitted state of the prior art teaches that the electrodes are used to provide connection to the electronic parts, and thus would connect with connecting devices or "pads" on the electronic parts. (3) (4) It further would have been obvious to modify Lin in view of the admitted state of the prior art to apply the oxidizing agent selectively to the non electrode portions (so that not all of the non-electrode portions are contacted with oxidizing agent) by a method such as ink jet printing as suggested by '623 and Miller in order to provide a further desirable selective overplating, as Lin in view of the admitted state of the prior art teaches to apply oxidizing agent to an entire surface so that non-conductive surfaces are not coated and '623 teaches that when overplating, there are times when it is desired to have coating over some of the non-conductive areas as well, and Miller provides a desirable method

for selectively applying materials for electroless plating to particular parts of the substrate is by ink jet printing. As this method would apply oxidizing agent in a predetermined pattern to some parts of the non-conductive surface and not apply oxidizing agent to other parts, oxidizing agent would be formed selectively in portions, which are smaller than a predetermined dimension, out of the space portion between the electrodes as claimed. As well, the oxidizing agent would be coated in a portion which is smaller than the overall "space portion" (all the areas between all the electrodes), because some space portion would not be coated with oxidizing agent. As to the oxidizing agent being selectively coated in areas between the electrodes of the conductive pattern that are less than 30 microns, one of ordinary skill in the art would optimize where to provide the overplating based on the specific use of the substrate desired, as '623 shows, for example, the plating of layers in desired particular areas of the substrate, and it would be obvious that some of the areas not plated would include areas of less than 30 microns, as all of the areas are not overplated. The use of the oxidizing agent as claimed would also provide for omitting the use of a solder resist, as the pattern is formed with oxidizing agent.

9. Claims 9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over EP 837 623 (hereinafter '623) in view of the admitted state of the prior art.

'623 teaches that it is well known to overplate by electroless plating selectively over conductive patterns on a insulating substrate when making printed circuit boards,

for example. Column 1, lines 1-10 and column 4, lines 35-45. The overcoating can be nickel based resistors. Column 7, lines 1-15. '623 provides providing a conductive circuit pattern on the insulating substrate. Column 4, lines 35-55. Then the surfaces of the conductive pattern and the substrate are activated by applying a catalytic metal serving as a catalyst for electroless plating. Column 4, lines 50-55 and column 6, lines 30-45. Then '623 provides applying a plating mask (protection film) onto the activated substrate so that the areas to be plated are defined in a negative manner, where the plating mask covers all or substantially all of the surfaces except for the resistor areas to be plated. Column 6, lines 45-55. The area to be plated can be partially over the conductive pattern and partially over the insulating substrate. Column 6, lines 50-56. Then, electroless plating occurs, with plating occurring only on the areas not covered by the mask. Column 7, lines 1-15. The exact size of the resistor area to be plated can vary. Column 7, lines 20-30.

Claim 9: the plating mask can be any typical plating mask known in the art. Column 6,lines 55-60.

It is the Examiner's position that resist films are well known in the art of electroless plating as plating masks. As applicant has not traversed this statement from the October 31, 2006 Office Action, it is understood to be agreed to.

'623 teaches all the features of these claims except that (1) the conductive pattern includes electrodes to be used with connection pads, (2) the space portion between the electrodes has a plurality of different values, (3) that the protection film is coated

selectively so that the protection film is formed selectively in portions, which are smaller than 30 microns, out of the space portion between the electrodes, (4) the protection film material (claim 9).

The admitted state of the prior art teaches that when forming wiring substrates with conductive patterns, it is well known for the wiring patterns to include electrodes formed of copper which then are overplated to enhance reliability, and the electrodes form connections to the electronic parts. See paragraphs [0002]—[0008] of the specification. It is also well known for the pitch of the copper electrodes on the wiring substrate to be narrowed to 60 microns or less. See paragraph [0004] of the specification. It is also well known for the space portions between the copper electrodes to vary over the substrate. See paragraph [0006] of the specification. It is also well known to desire to form a nickel layer selectively on the copper electrodes by electroless plating. See paragraphs [0002]—[0008] of the specification.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to (1) (2) modify '623 to provide that the conductive pattern includes electrodes spaced different distances apart as suggested by the admitted state of the prior art in order to provide a desirable circuit pattern because '623 teaches forming conductive patterns on insulating substrates for circuit usage, and the admitted state of the prior art teaches that conductive patterns on wiring substrates for such purposes conventionally have copper electrodes spaced different distances apart. As to the electrodes being on which connection pads of an electronic part are connected, the

admitted state of the prior art teaches that the electrodes are used to provide connection to the electronic parts, and thus would connect with connecting devices or "pads" on the electronic parts. (3) It further would have been obvious to modify '623 in view of the admitted state of the prior art to apply the protection film selectively to the non electrode portions (so that not all of the non-electrode portions are contacted with film) in order to provide a further desirable selective overplating, as '623 teaches that when overplating, there are times when it is desired to have coating over some of the non-conductive areas as well. As this method would apply the protection film in a predetermined pattern to some parts of the non-conductive surface and not apply protection film to other parts, protection film would be formed selectively in portions, which are smaller than a predetermined dimension, out of the space portion between the electrodes as claimed. As well, the protection film would be coated in a portion which is smaller than the overall "space portion" (all the areas between all the electrodes), because some space portion would not be coated with protection film. As to the protection film being selectively coated in areas between the electrodes of the conductive pattern that are less than 30 microns, it further would have been obvious to perform routine experimentation to optimize the distance apart to less than 30 microns apart in at least some cases as the admitted state of the prior art provides that less than 60 microns apart is conventional, and 30 microns is included in the range of less than 60 microns. Furthermore, one of ordinary skill in the art would optimize where to provide the overplating based on the specific use of the substrate desired, as '623 shows,

for example, the plating of layers in desired particular areas of the substrate, and it would be obvious that some of the areas not plated would include areas of less than 30 microns, as all of the areas are not overplated. The use of the protection film as claimed would also provide for omitting the use of a solder resist, as the pattern is formed with plating mask. (4) it would further have been obvious to modify '623 in view of the admitted state of the prior art to use a resist film as the protection film material with an expectation of desirable coating results, because '623 teaches to use any typical plating mask known in the art, and it is the Examiner's position that a resist film is well known in the art as a plating mask.

*Response to Arguments*

10. Applicant's arguments filed May 23, 2007 have been fully considered but they are not persuasive.

(A) Applicant argues, as to the rejection of claims 1, 3, 4, 7 and 10 using Lin in view of the admitted state of the prior art, '623 and Miller, that none of the cited references teaches, mentions or suggests that the oxidizing agent is selectively coated in portions, which are smaller than both a predetermined value and the distance between electrodes, where the distance between electrodes in the space portion between the electrodes has a plurality of different values. Applicant argues that, in particular, "when a metal layer is selectively formed on the conductive pattern by electroless plating, because an electric short-circuit can easily occur in the narrow space portions

(especially space portions smaller than 30 μm), the oxidizing agent or the protective film should be formed in the space portions in which the distance between electrodes is smaller than a predetermined distance where the electric short-circuit may easily occur." Applicant notes that the references do not note the problems with short circuits and the problems with solder resist on small space portions.

The Examiner has reviewed these arguments, however, the rejection is maintained. Applicant appears to be arguing that the references do not teach or suggest applying the oxidizing agent specifically in spaces measured between conductive electrodes that are less than 30 microns (or other predetermined dimensions) in order to prevent short circuits. However, this is not what is claimed. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Here all that is required is that the oxidizing agent is selectively coated in space portions that are smaller than 30 microns not that all such space portions are coated with the agent or that oxidizing agent only be applied in these portions. There is no indication as to the prevention of short circuits in the claims. Thus, applying the agent over some portions smaller than 30 microns reads on the claims as worded. Therefore, the suggestion of coating a protective material to provide masking (in this case the oxidizing agent) provided by the combination of references would be on an area that meets the claimed requirements. Moreover, as to the solder resist omission, this would

be provided by the combination of references which provides the suggestion of using the oxidizing agent.

(B) As to the rejection of claims 9 and 11 using '623 view of the admitted state of the prior art, applicant does not provide specific arguments as to these rejections, beyond that which would apply to claim 1 above. The Examiner maintains the rejection of these claims for the reasons given in (A) above, therefore.

*Interview*

11. As to the requested interview if the amendment did not place the case in condition for allowance, the Examiner did not have time before this Office Action was required to be provided and mailed to provide for an interview based on the above discussed reasons for maintaining the rejection. Moreover, the Examiner believes that the issues were not ripe for interview because applicant would not have been able to see and review the Examiner's response to the May 23, 2007 arguments before an interview, thus making for a confusing interview and discussion of the case. If after review of this Office Action applicant still desires an interview, applicant is requested to contact the Examiner at the contact number provided in the ***Conclusion*** section below.

*Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Katherine A. Bareford whose telephone number is (571)

272-1413. The examiner can normally be reached on M-F(6:00-3:30) with the First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Meeks can be reached on (571) 272-1423. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and for After Final communications.

Other inquiries can be directed to the Tech Center 1700 telephone number at (571) 272-1700.

Furthermore, information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KATHERINE BAREFORD
PRIMARY EXAMINER